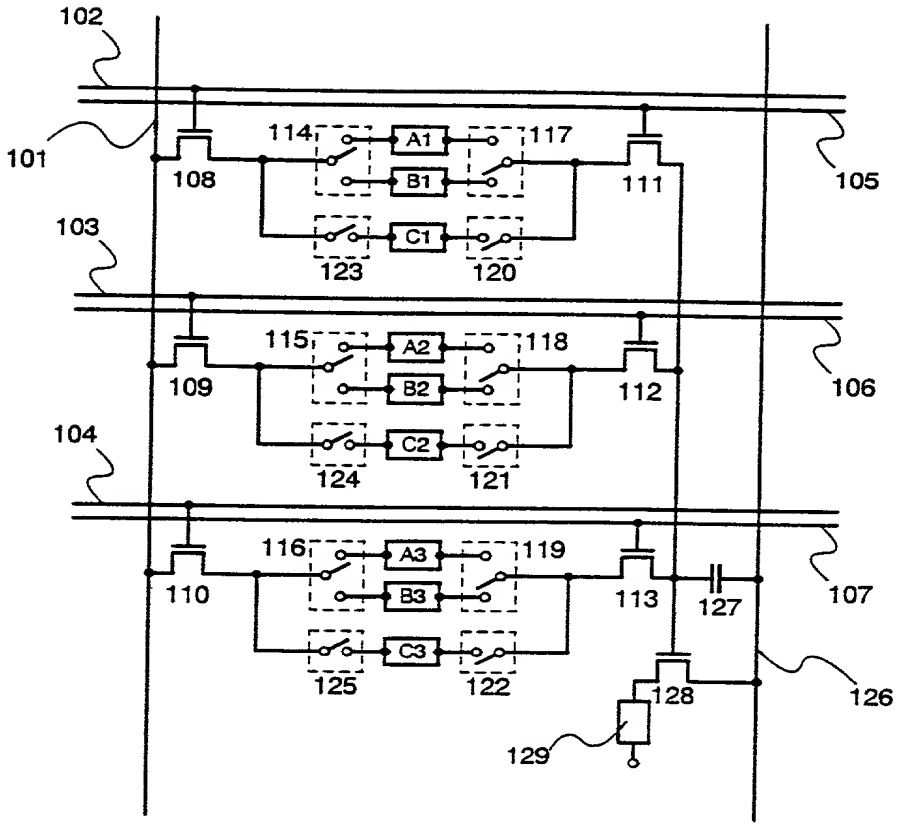
Fig. 1


102
101
114
A1
117
108
B1
111
105
C1
123
120
103
115
A2
118
109
B2
112
106
C2
124
121
104
116
A3
119
110
B3
113
127
107
C3
125
122
128
126
129

EP 2 180 470 A1

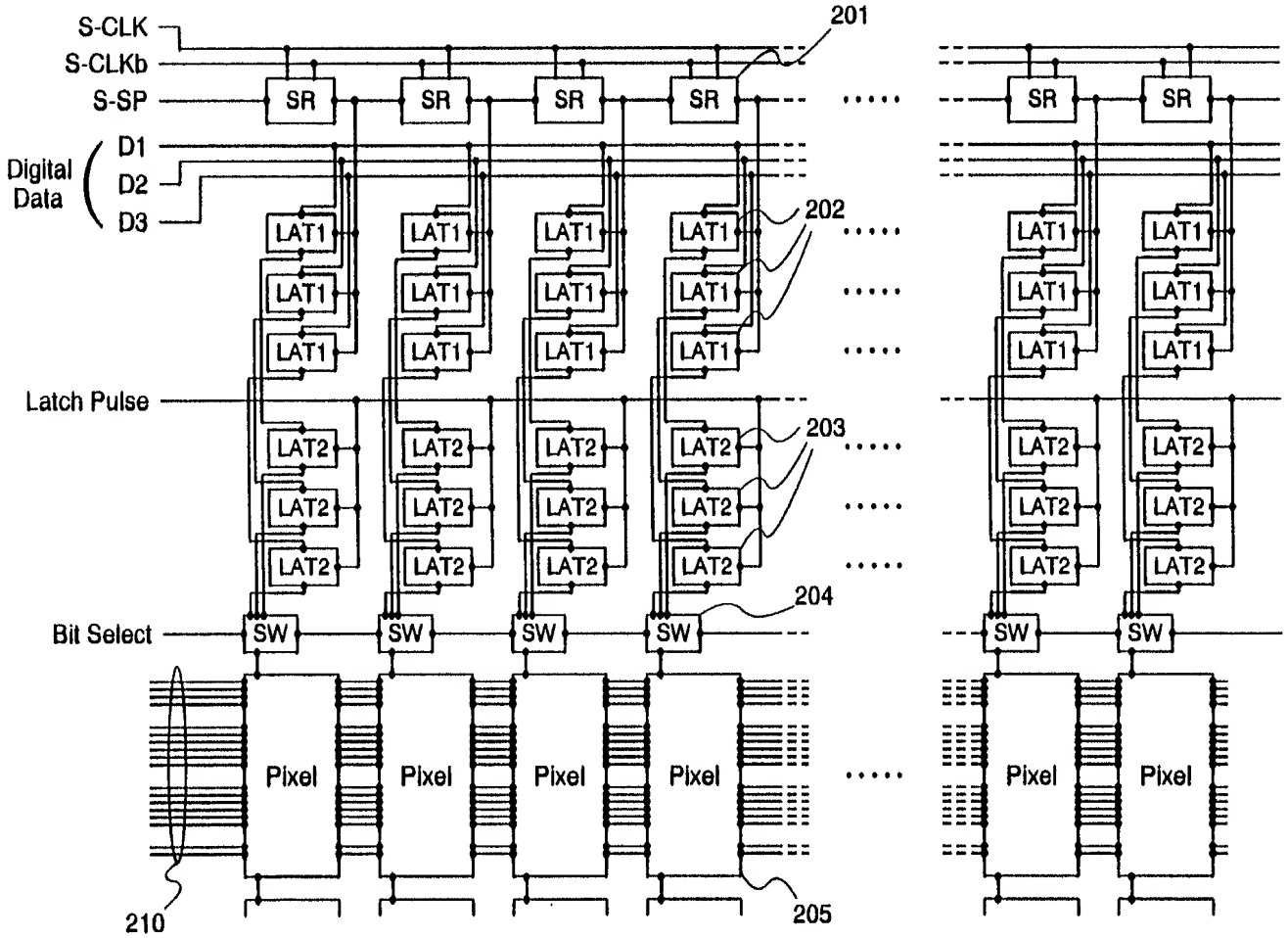


Fig. 2

TOSHIBA TSUTSUMI

Fig.3A

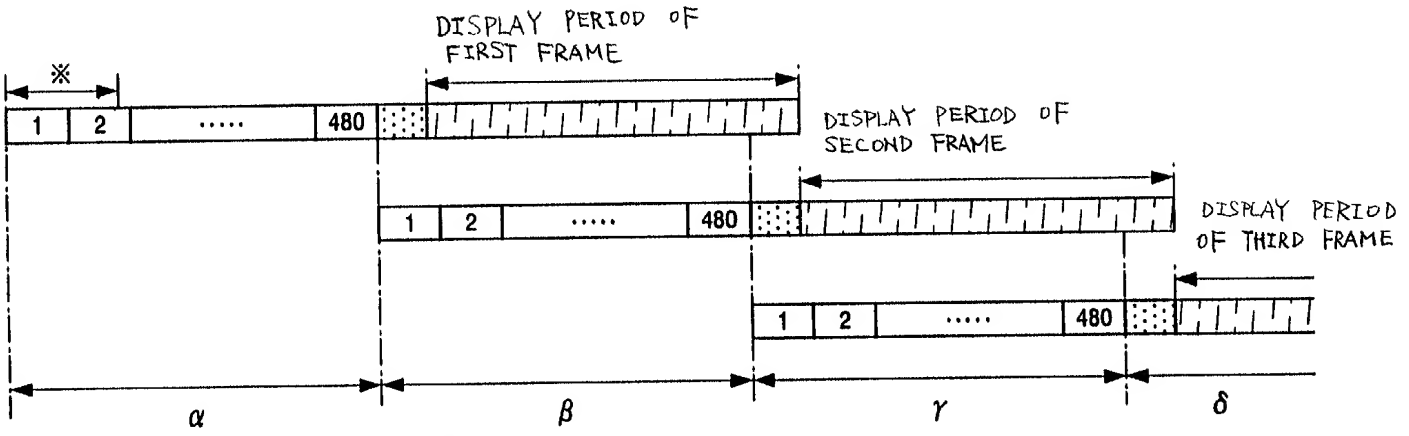


Fig.3B

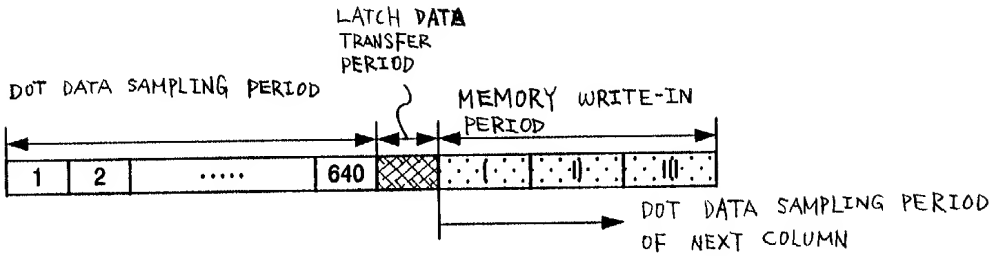


Fig.3C

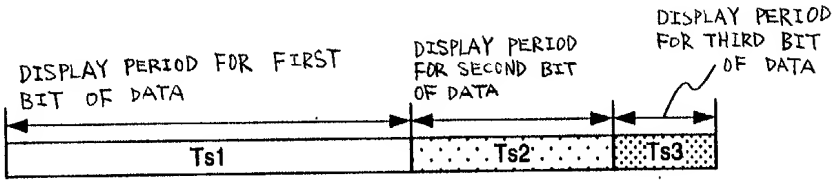
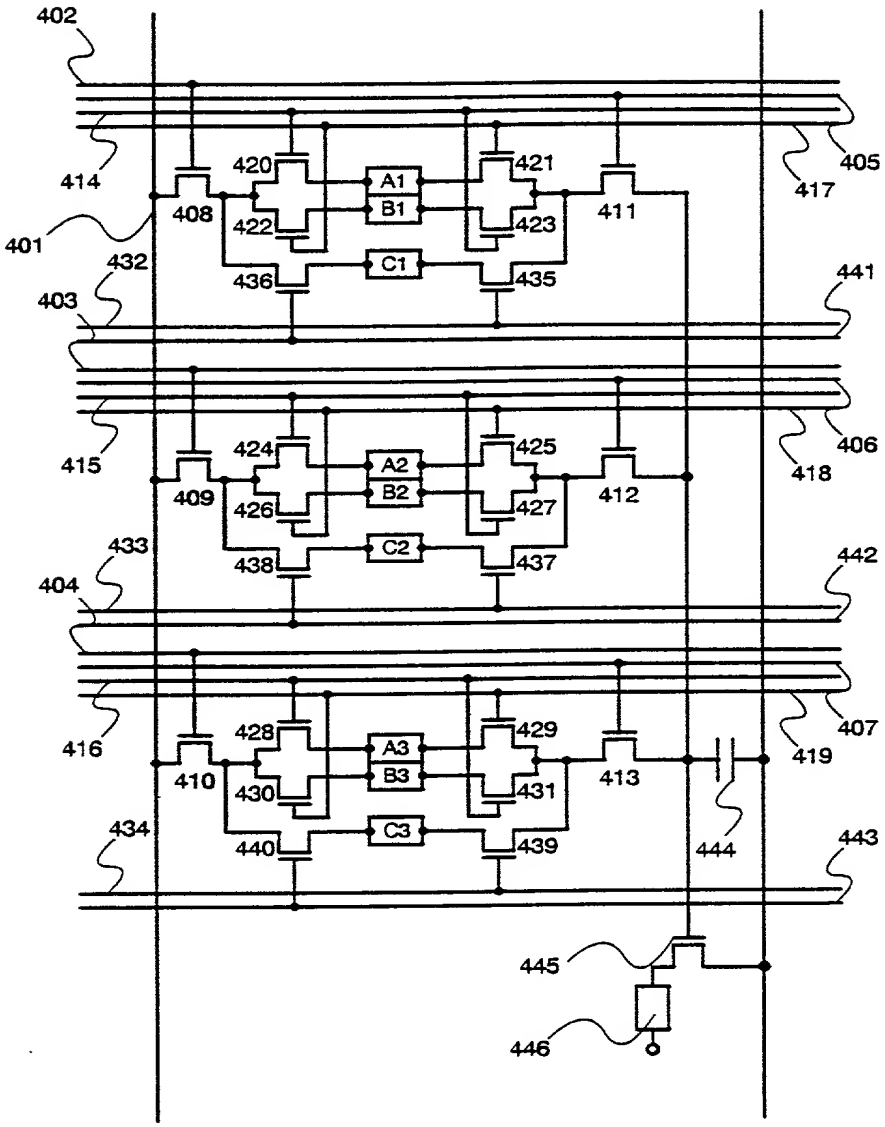


Fig. 4



401 : SOURCE SIGNAL LINE
444 : STORAGE CAPACITOR (C_S)
445 : EL DRIVER TFT (NV)

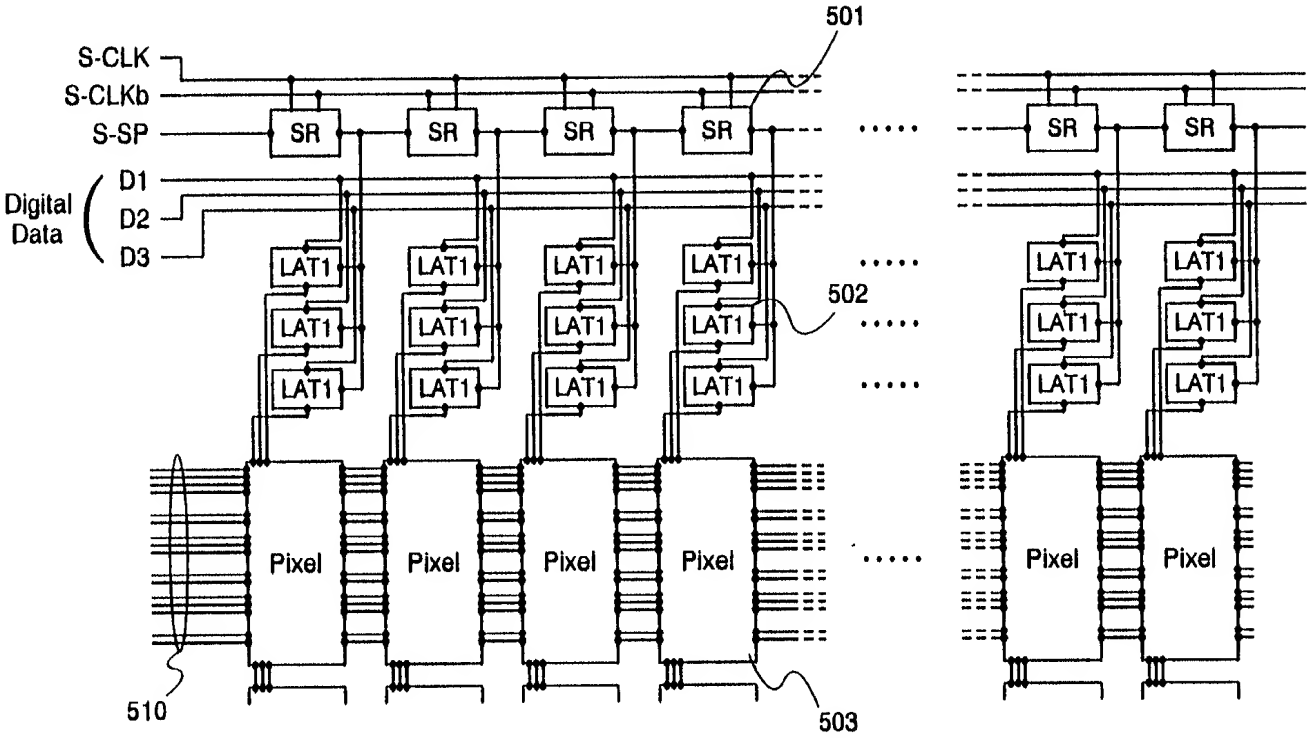
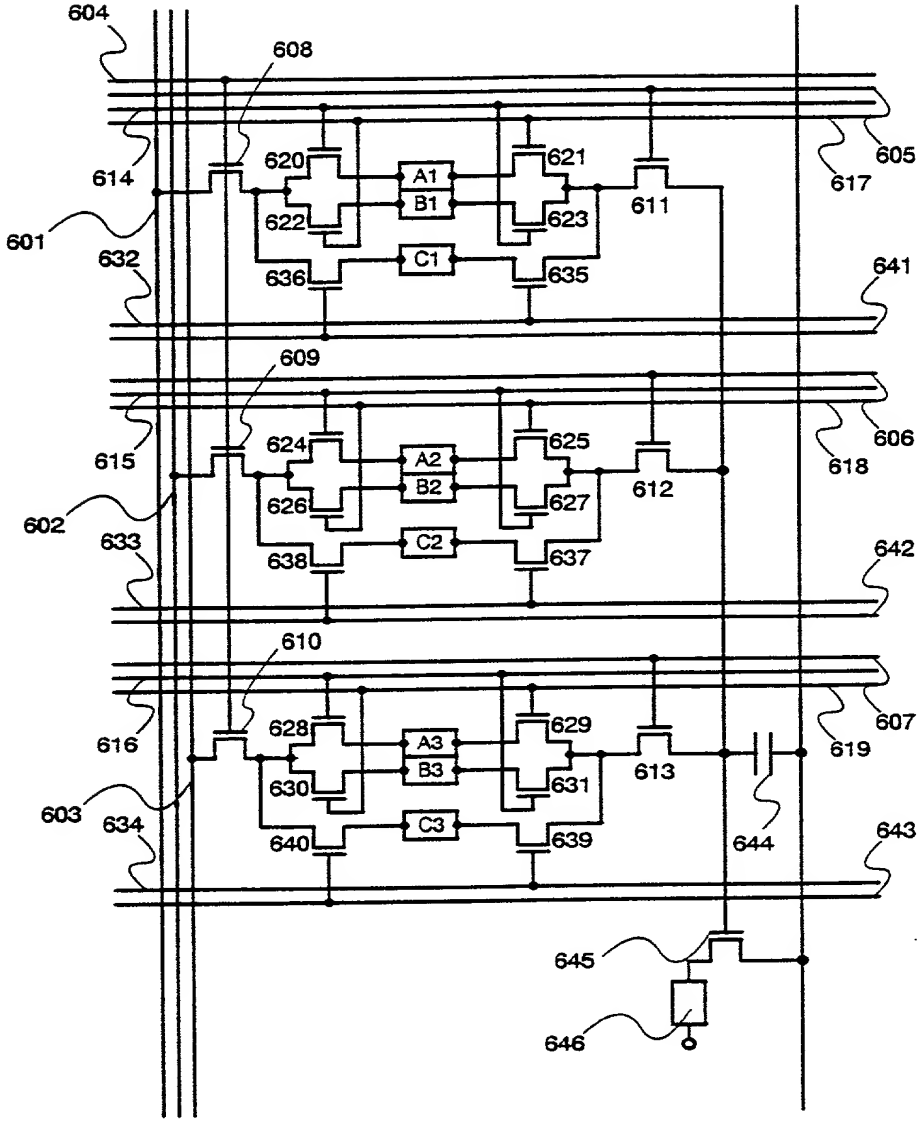

501
S-CLK
S-CLKb
S-SP
Digital Data
D1
D2
D3
SR
LAT1
502
Pixel
510
503

Fig. 5

Fig. 6


604
608
614
620
621
A1
B1
605
617
601
622
623
611
632
C1
636
635
641
609
615
624
625
A2
606
618
602
626
B2
627
612
633
C2
638
637
642
610
616
628
629
A3
607
619
603
630
B3
631
613
634
C3
640
639
644
643
645
646

FUJITSU-1001-2600

Fig. 7A

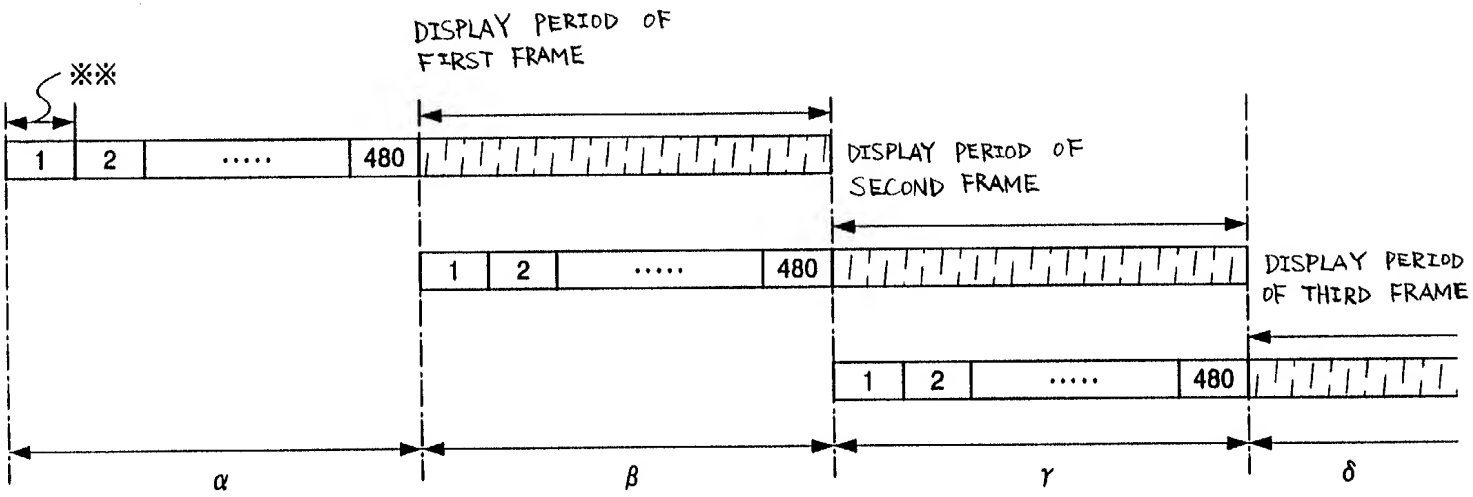


Fig. 7B

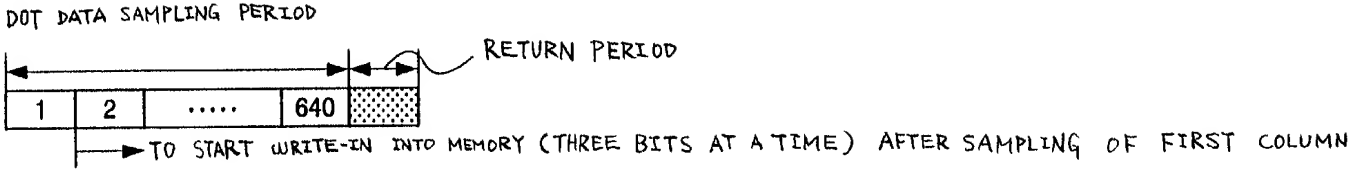


Fig. 7C

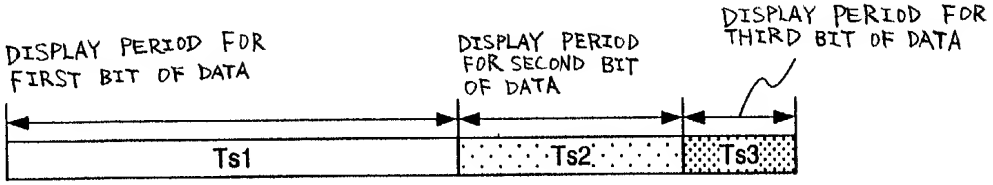
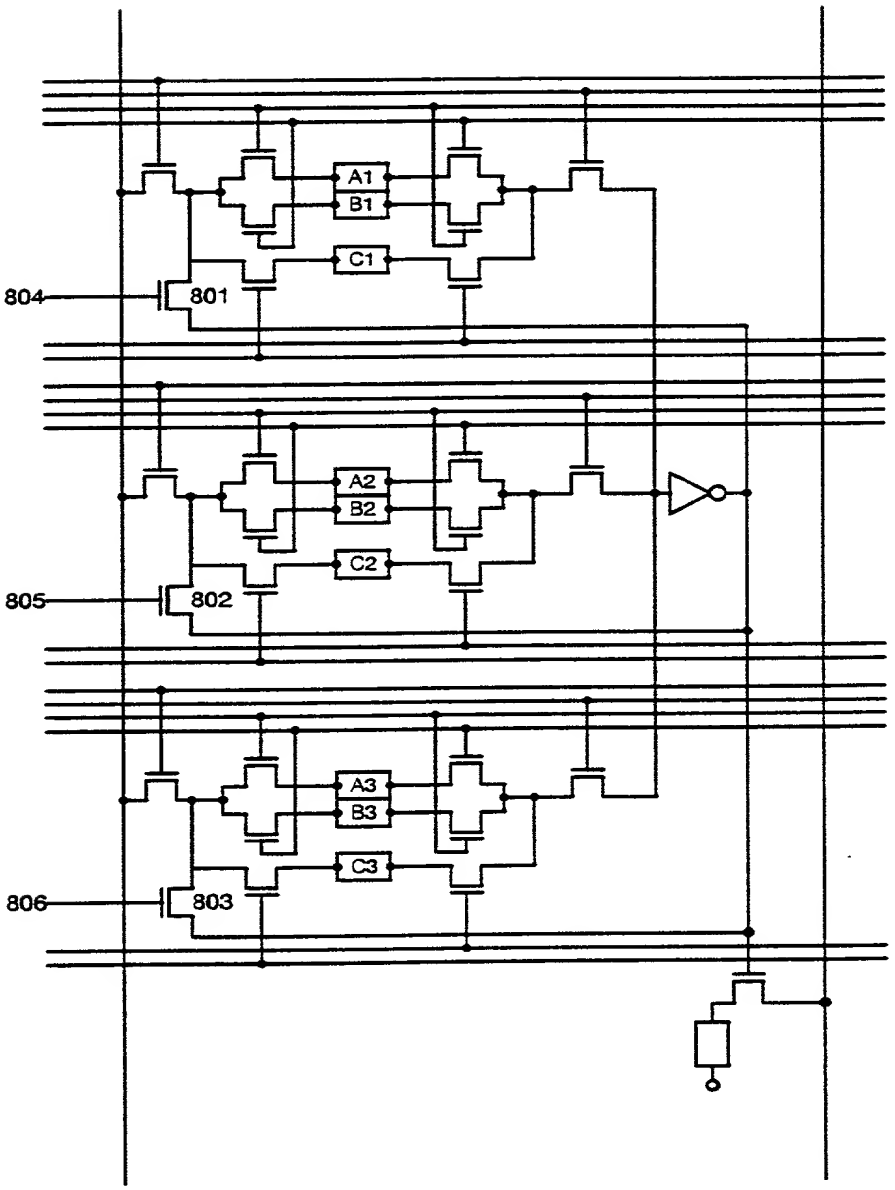


Fig. 8



804~806 : REFRESHING SIGNAL LINE

Fig. 9A

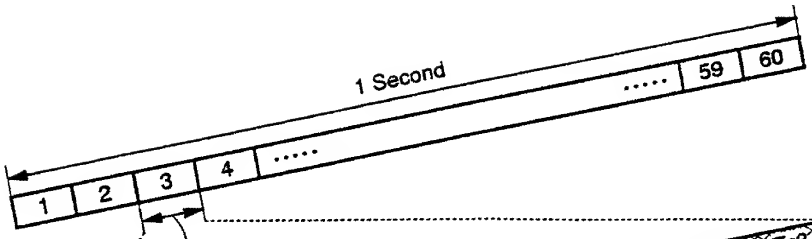


Fig. 9B

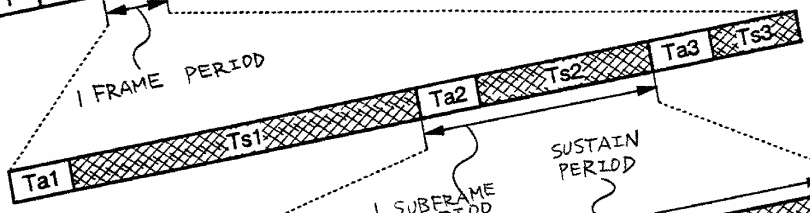


Fig. 9C

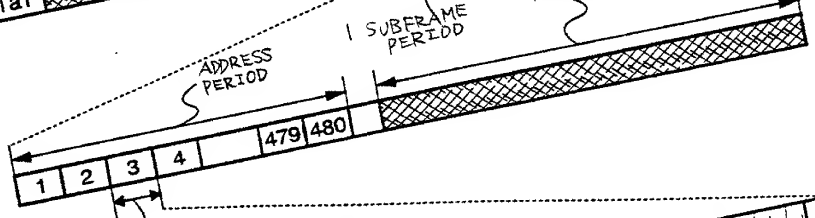
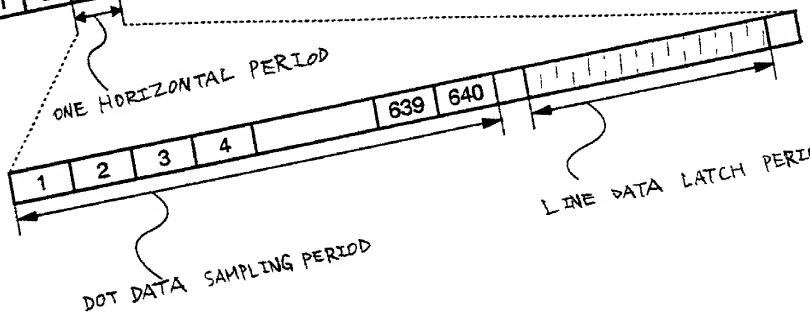


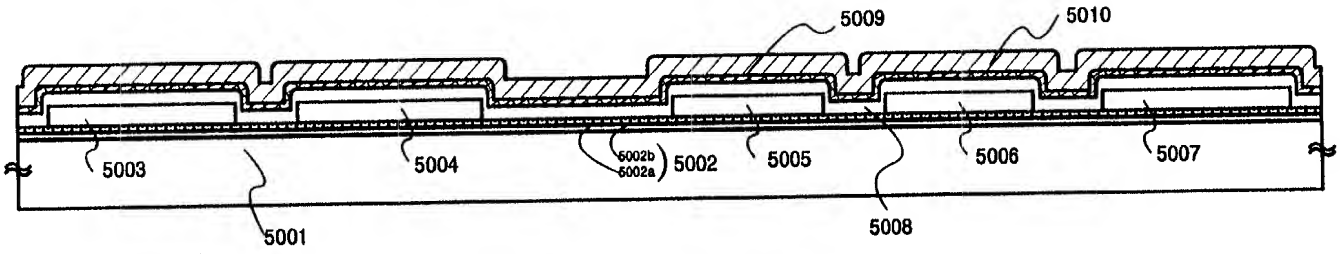
Fig. 9D



EXCEL TECHNOLOGY

FORMATION OF ISLAND-LIKE SEMICONDUCTOR FILM AND GATE INSULATING FILM AND FIRST AND SECOND CONDUCTIVE FILMS FOR GATE ELECTRODE

Fig.10A



FIRST ETCHING PROCESS AND FIRST DOPING PROCESS

Fig.10B

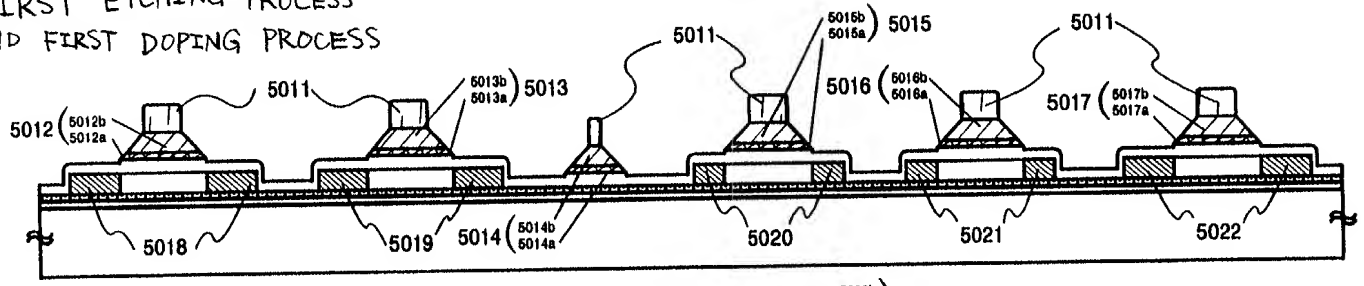


Fig.10C) SECOND ETCHING PROCESS

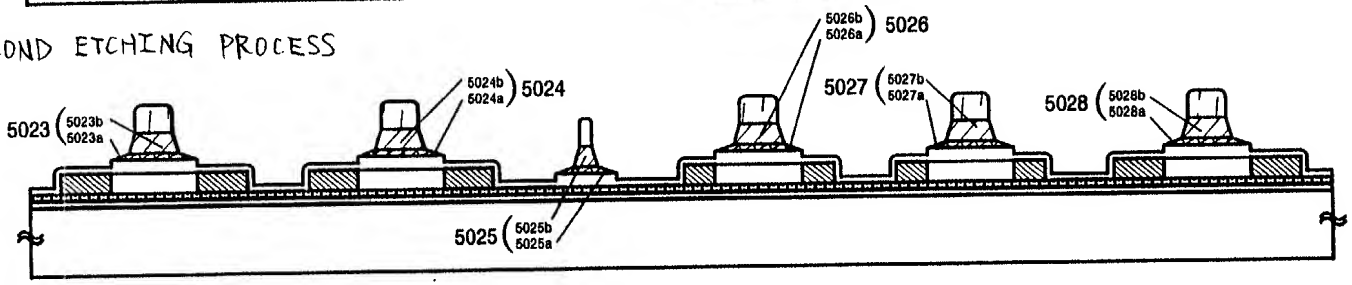


Fig.11A SECOND DOPING PROCESS

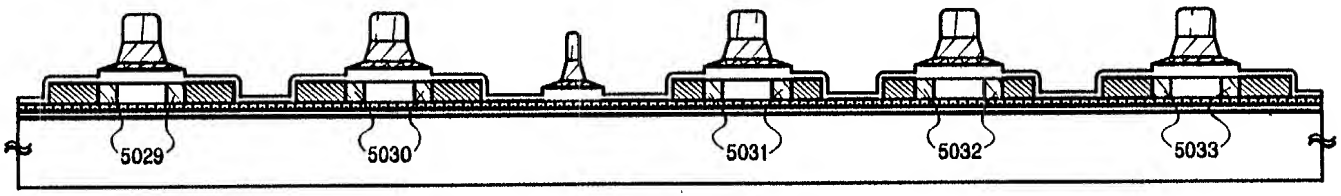


Fig.11B THIRD ETCHING PROCESS

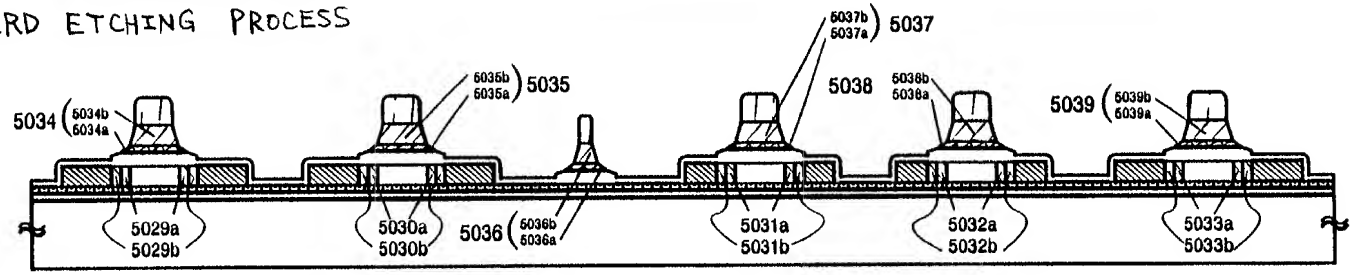
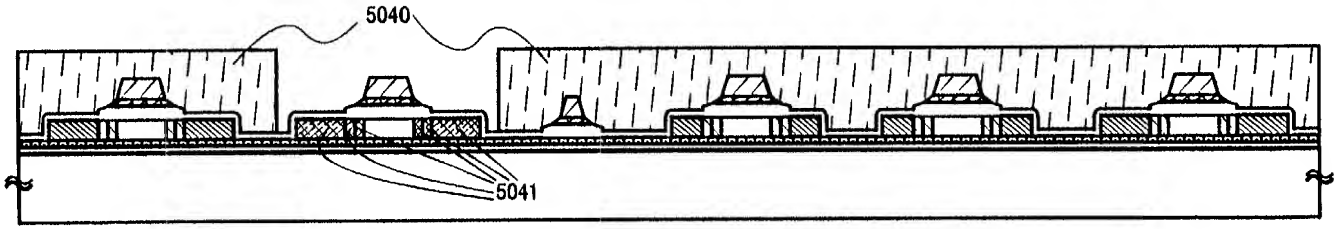
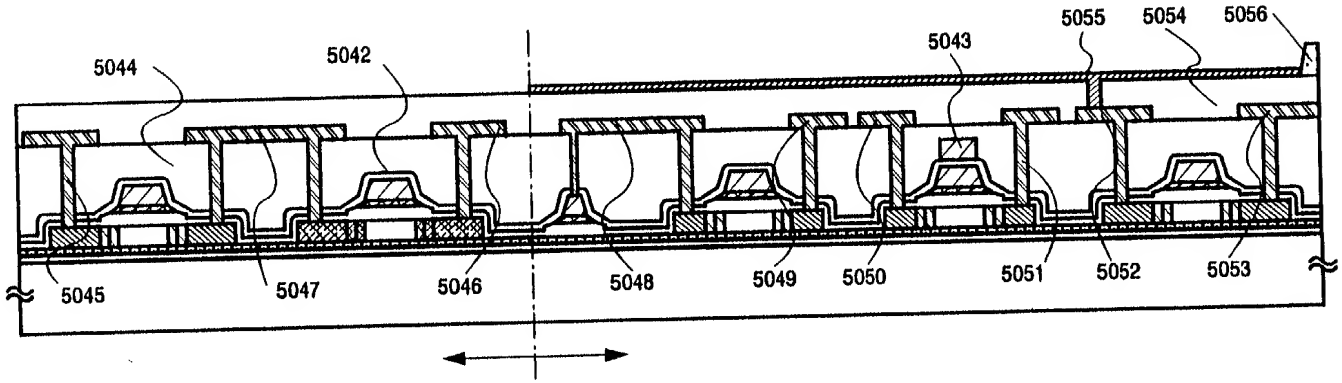


Fig.11C THIRD DOPING PROCESS



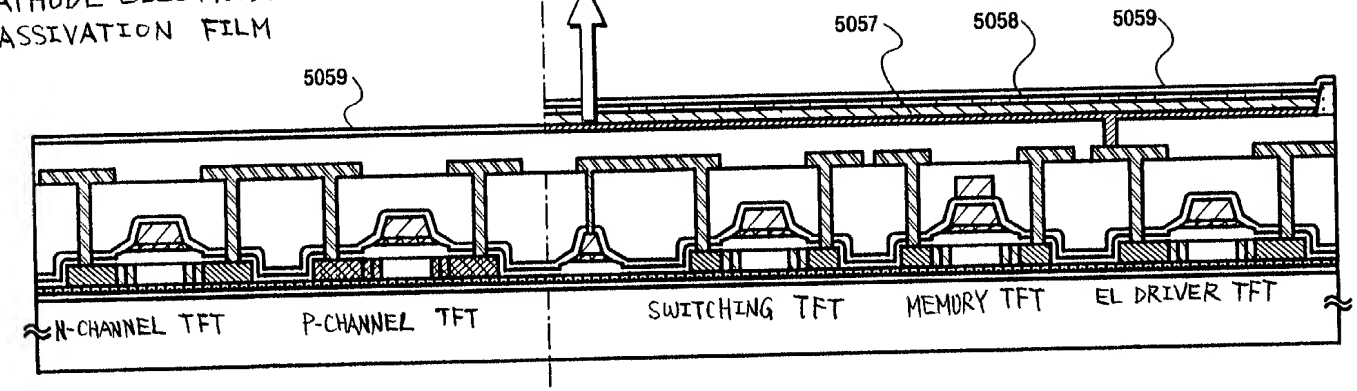
FORMATION OF SECOND GATE INSULATING FILM AND CONTROL GATE AND FIRST INTERLAYER INSULATING FILM AND WIRING AND SECOND INTERLAYER INSULATING FILM AND PIXEL ELECTRODE

Fig.12A



FORMATION OF EL LAYER AND CATHODE ELECTRODE AND PASSIVATION FILM

Fig.12B



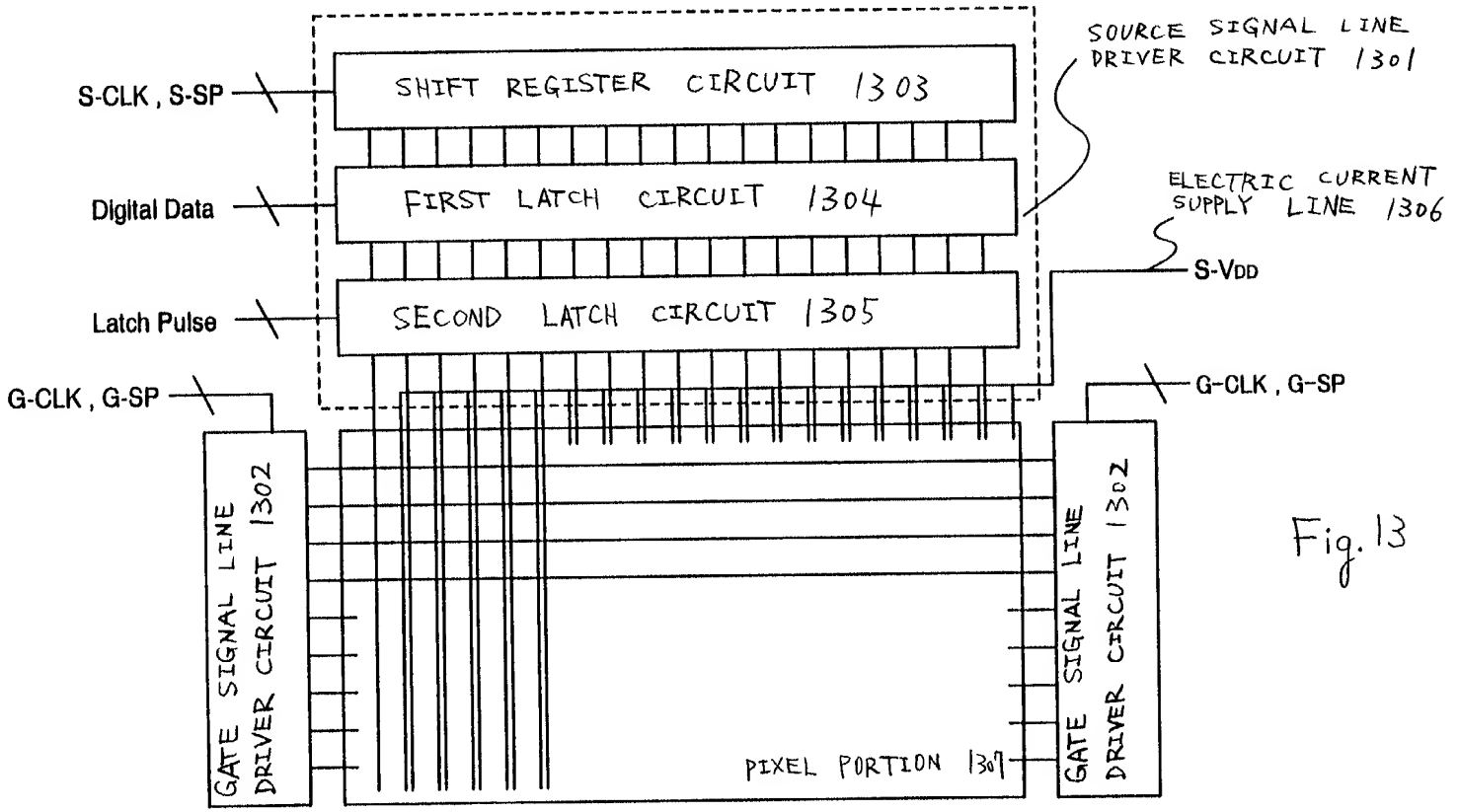

SOURCE SIGNAL LINE DRIVER CIRCUIT 1301
SHIFT REGISTER CIRCUIT 1303
FIRST LATCH CIRCUIT 1304
SECOND LATCH CIRCUIT 1305
S-CLK , S-SP
Digital Data
Latch Pulse
G-CLK , G-SP
ELECTRIC CURRENT SUPPLY LINE 1306
S-VDD
G-CLK , G-SP
GATE SIGNAL LINE DRIVER CIRCUIT 1302
GATE SIGNAL LINE DRIVER CIRCUIT 1302
PIXEL PORTION 1307

Fig. 13

TOSHIBA TSU2000

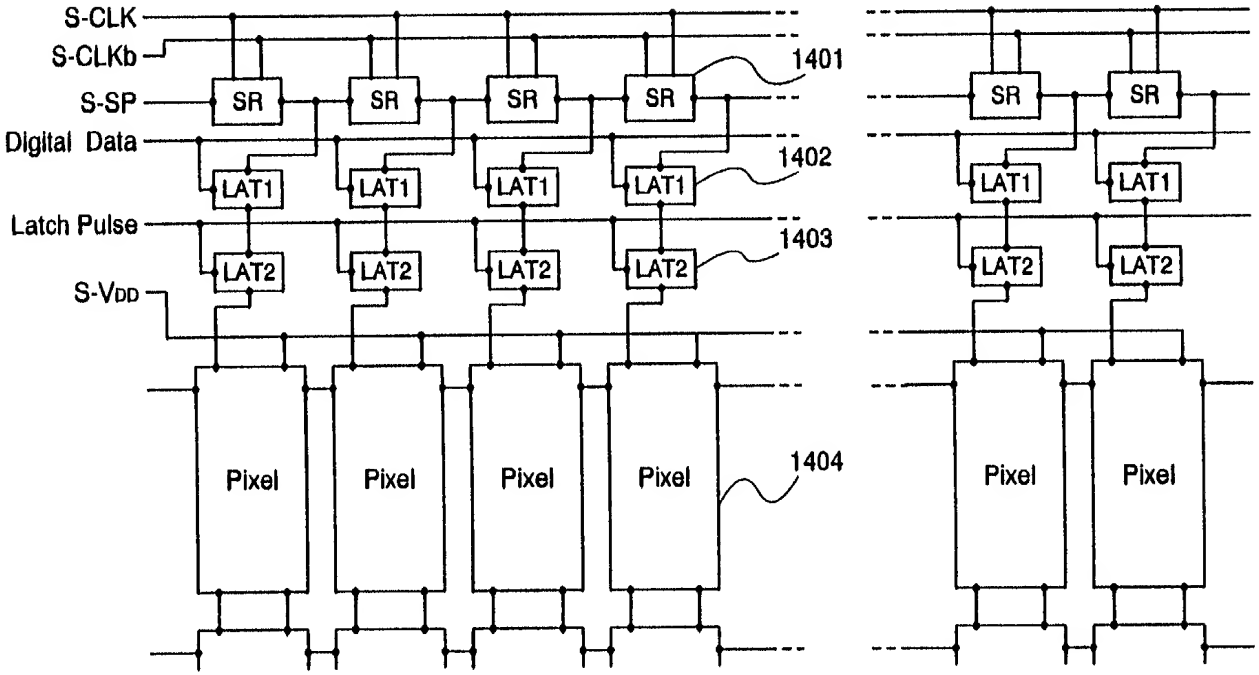


Fig.14

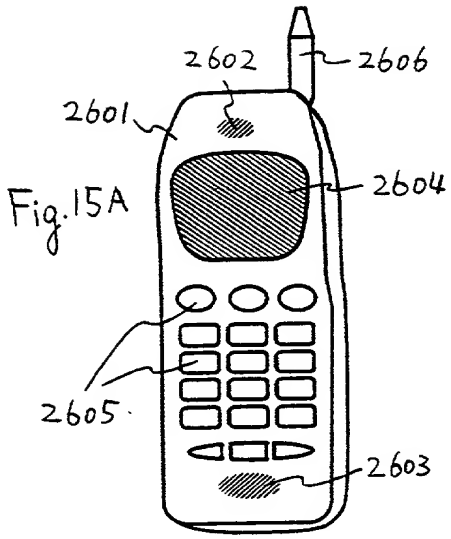


Fig.15A

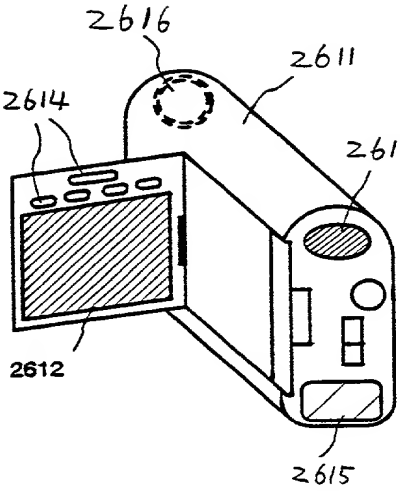


Fig.15B

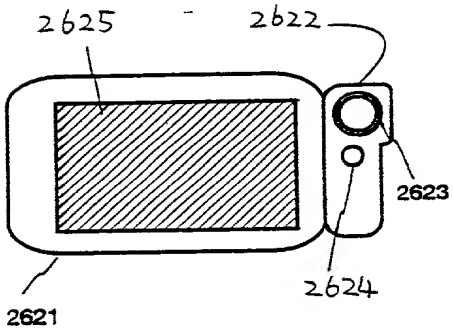


Fig.15C

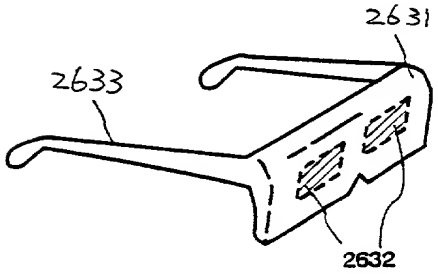


Fig.15D

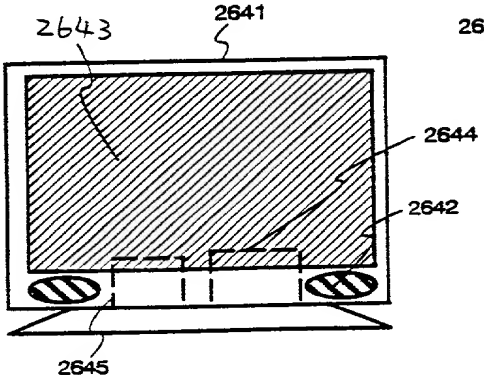


Fig.15E

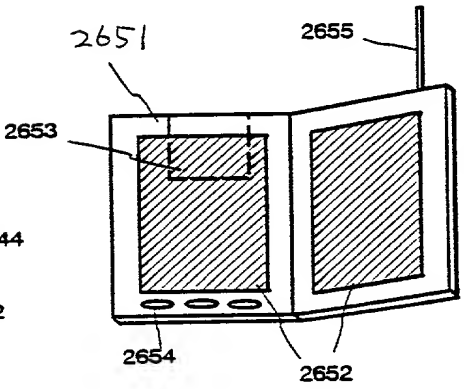


Fig.15F

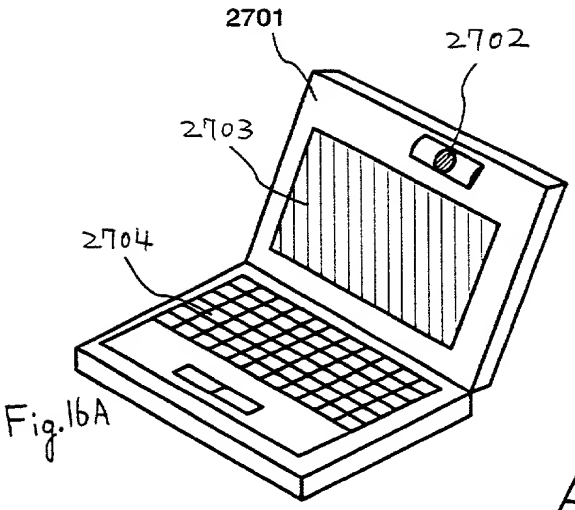


Fig.16A

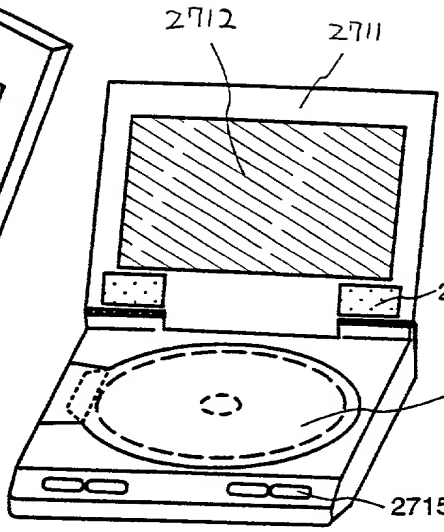


Fig.16B

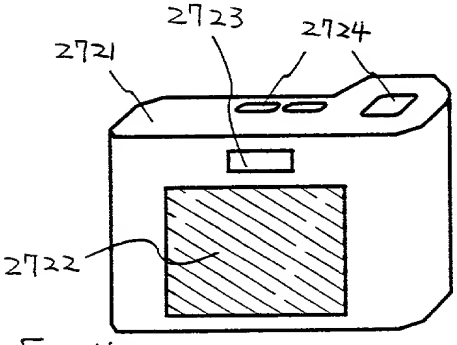


Fig.16C

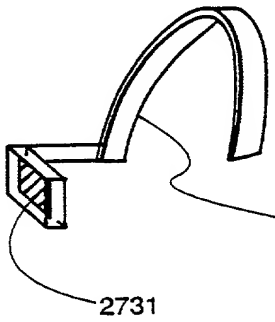


Fig.16D

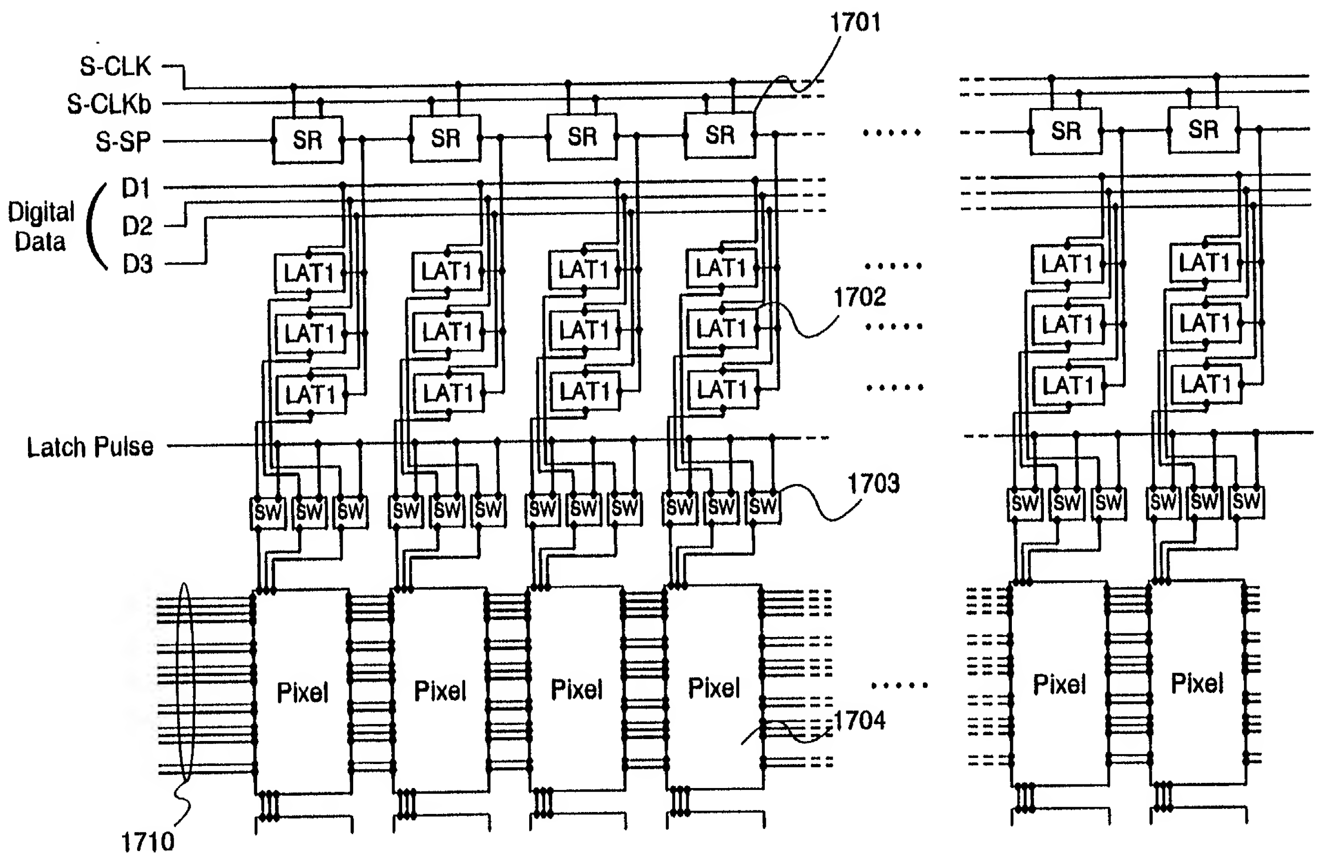

S-CLK
S-CLKb
S-SP
Digital Data
D1
D2
D3
Latch Pulse
SR
LAT1
SW
Pixel
1701
1702
1703
1704
1710

Fig. 17

Fig.18A

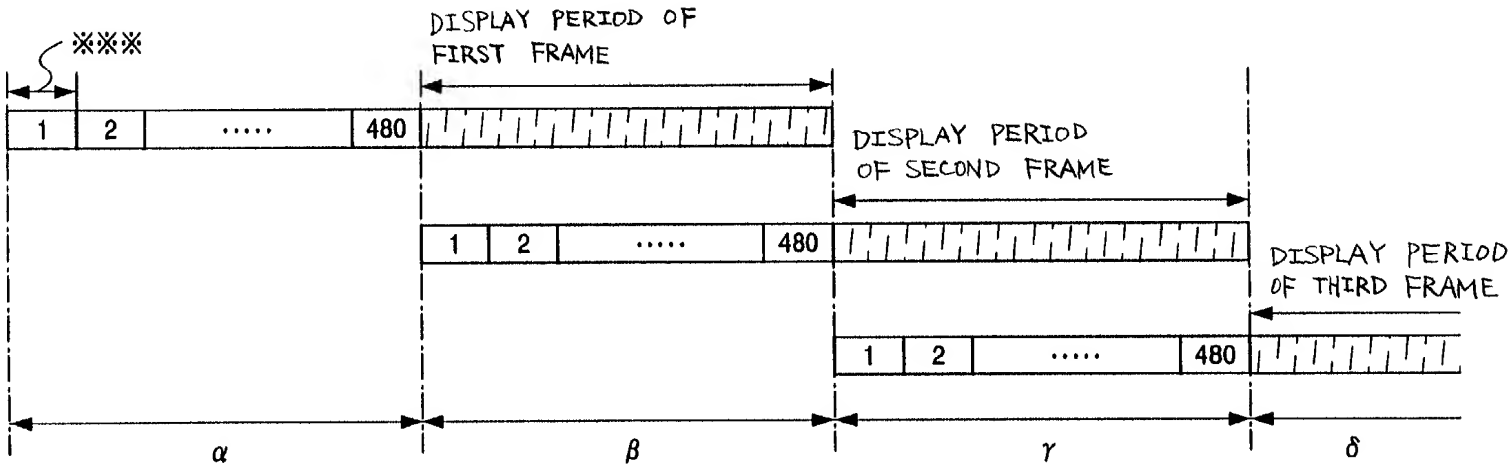


Fig.18B

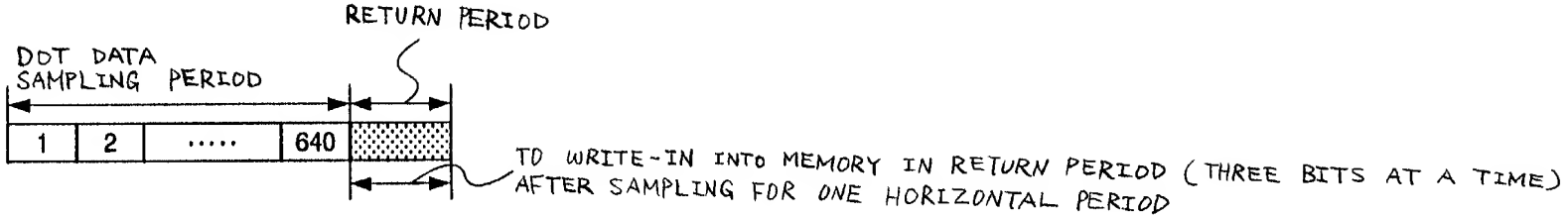


Fig.18C

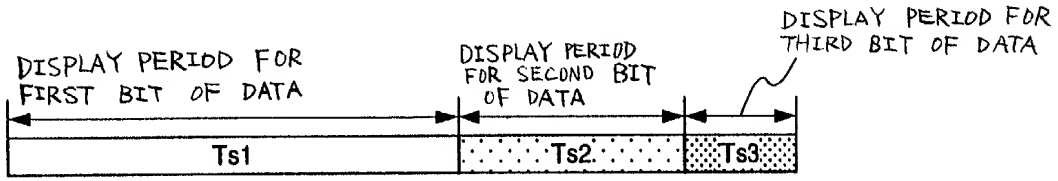


Fig. 19A

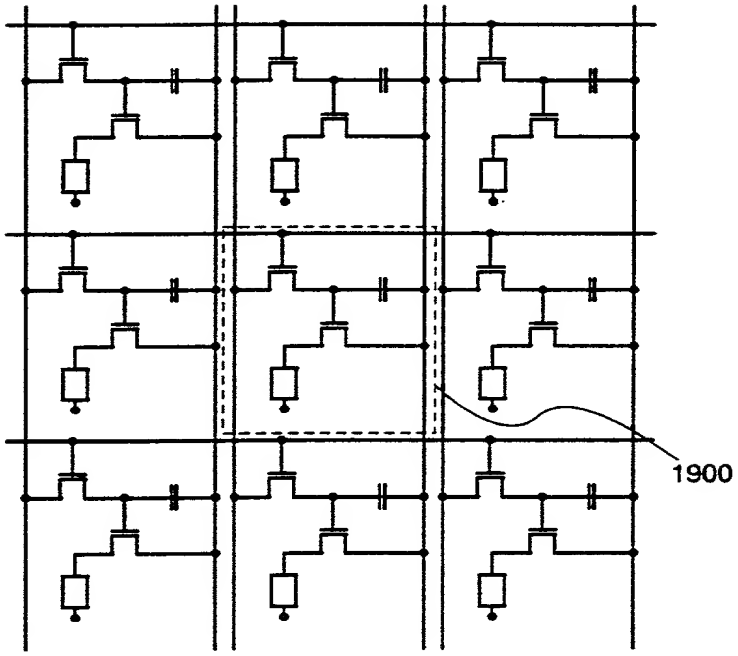


Fig. 19B

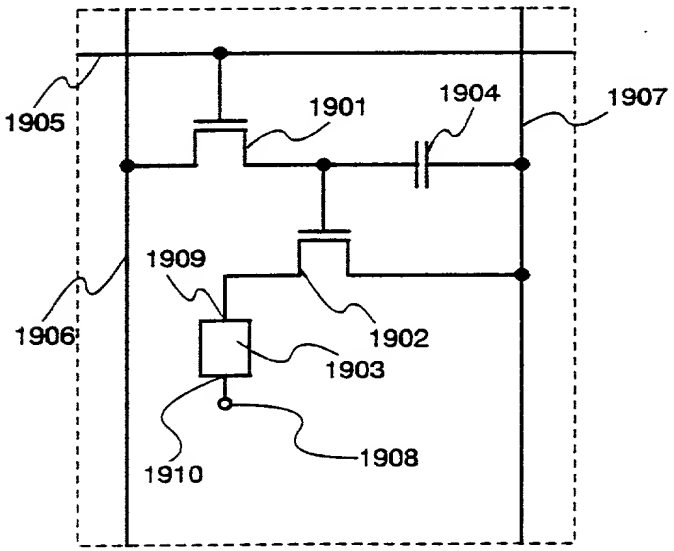


Fig. 20

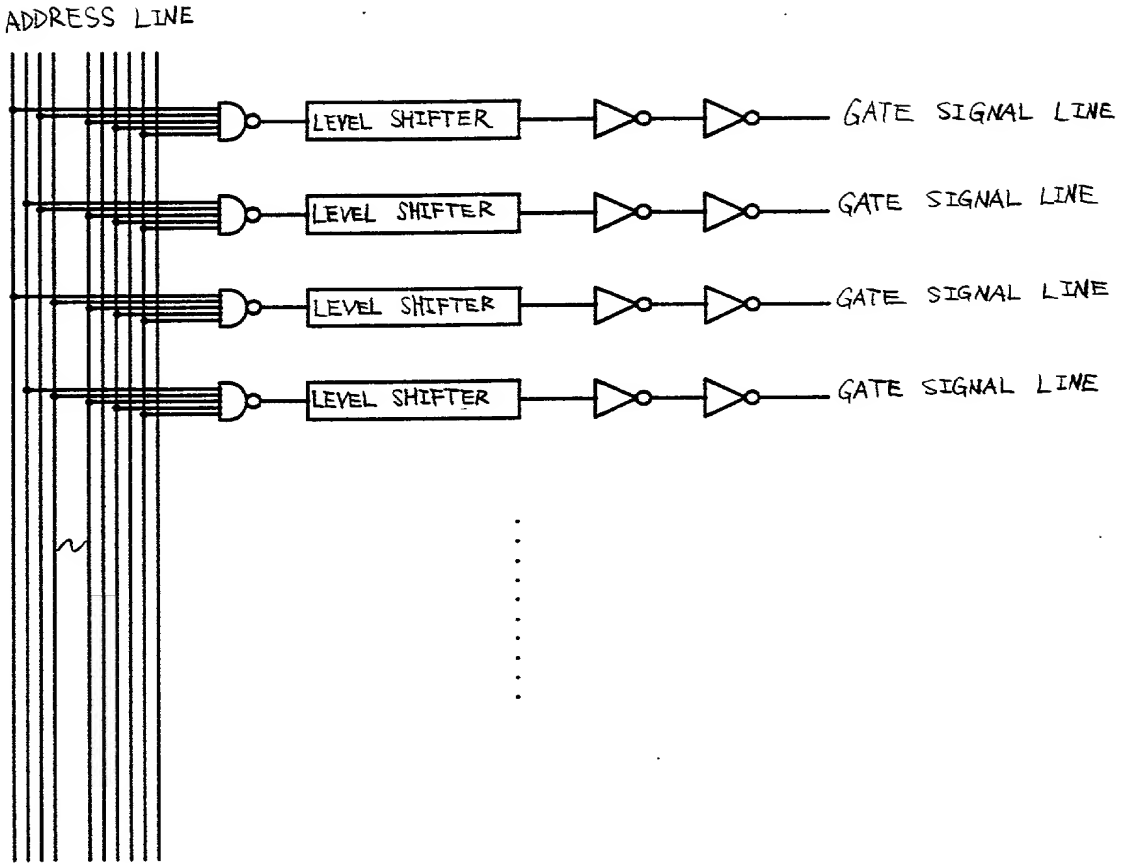
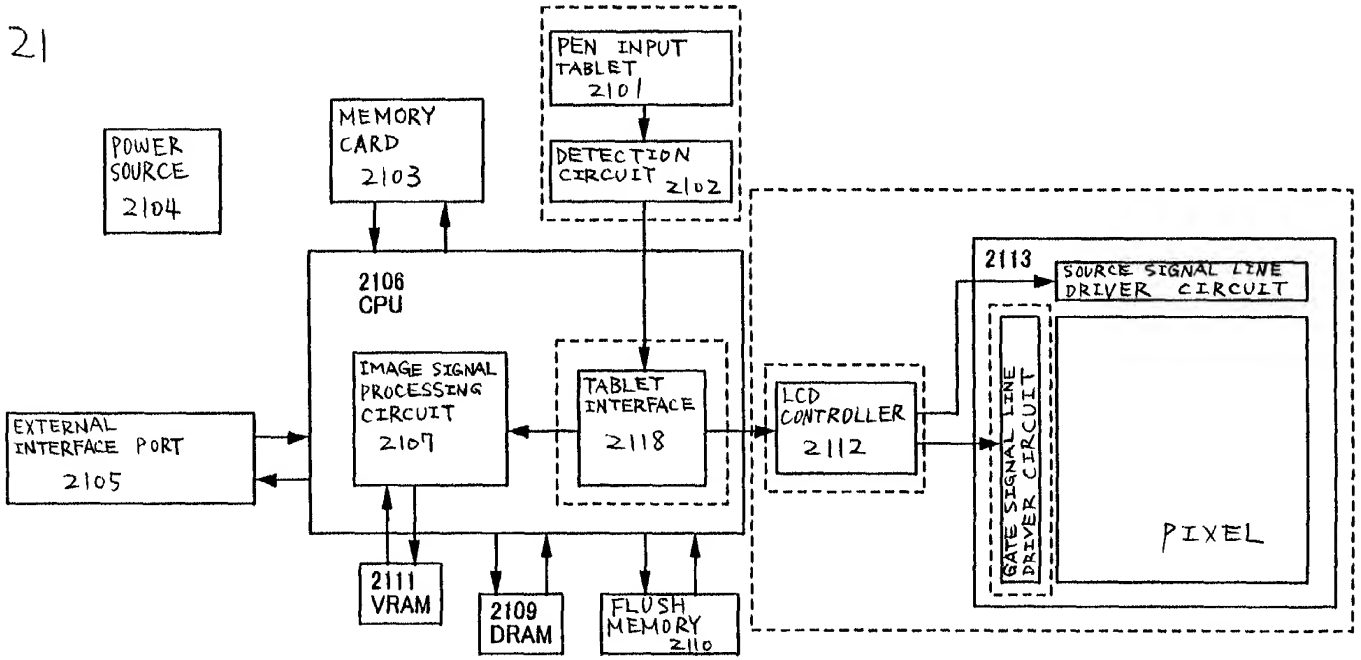

ADDRESS LINE
LEVEL SHIFTER
LEVEL SHIFTER
LEVEL SHIFTER
LEVEL SHIFTER
GATE SIGNAL LINE
GATE SIGNAL LINE
GATE SIGNAL LINE
GATE SIGNAL LINE

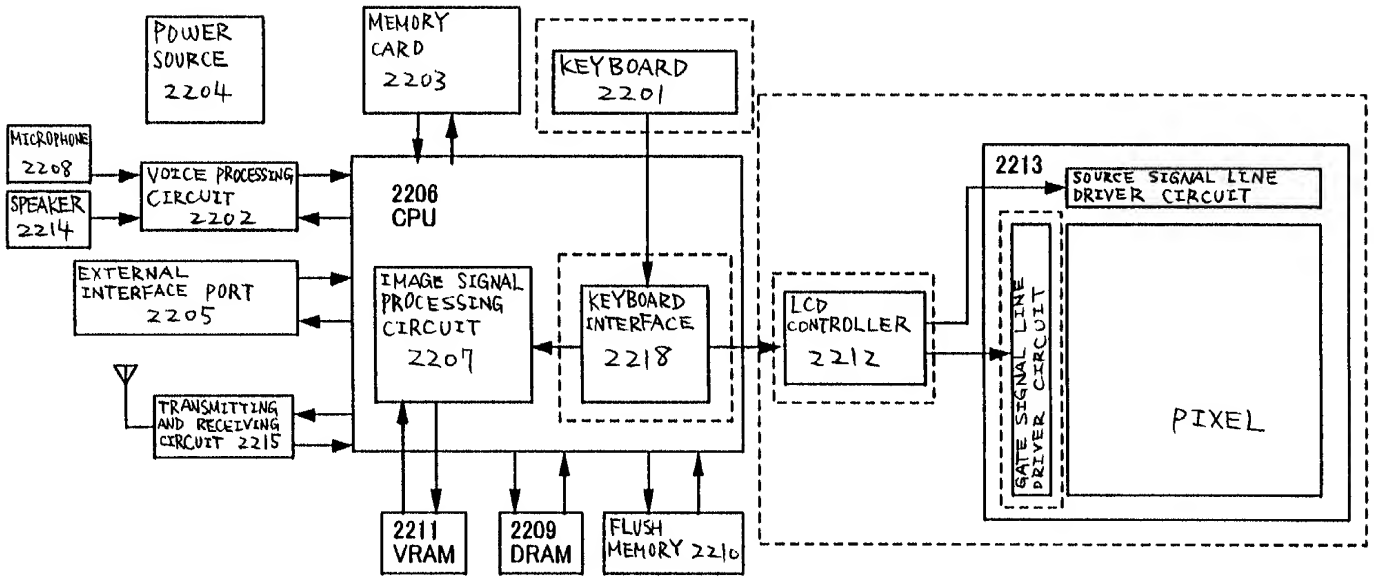
Fig. 21



BLOCK DIAGRAM OF PORTABLE INFORMATION TERMINAL

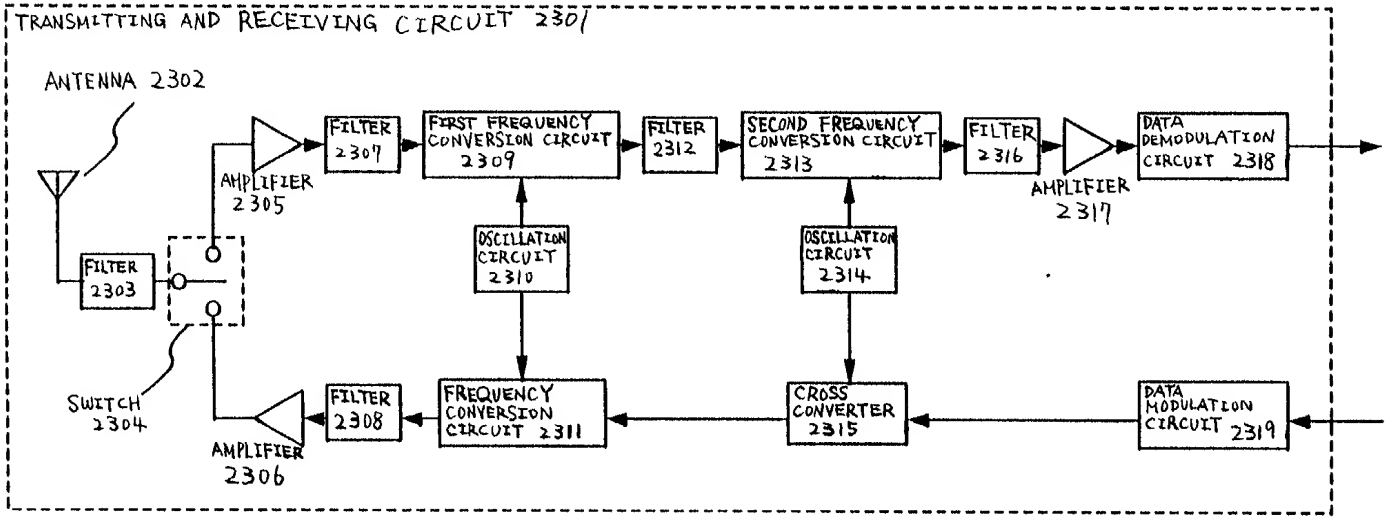
FOCTED: 13012000

Fig. 22



BLOCK DIAGRAM OF MOBILE TELEPHONE

Fig.23



BLOCK DIAGRAM OF TRANSMITTING AND RECEIVING CIRCUIT